10-19-00 A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Leonard Forbes et al.

Title: TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE

Attorney Docket No.: 303.324US4

PATENT APPLICATION TRANSMITTAL

BOX PATENT APPLICATION
Commissioner for Patents
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We are transmitting herewith the following attached items and information (as indicated with an "X"):

X Return postcard.
X **CONTINUATION** of prior Patent Application No. 08/903,452 (under 37 CFR § 1.53(b)) comprising:
  X Specification (32 pgs, including claims numbered 1 through 35 and a 1 page Abstract).
  X Formal Drawing(s) (11 sheets).
  X Signed Combined Declaration and Power of Attorney (6 pgs).
  X Incorporation by Reference: *The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied herewith, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.*
  X Check in the amount of $2,800.00 to pay the filing fee.
X Prior application is assigned of record to Micron Technology, Inc. .
X Information Disclosure Statement (1 pgs), Form 1449 (10 pgs). References NOT enclosed, cited in prior application.
X Preliminary Amendment (16 pgs).

The filing fee has been calculated below as follows:

	No. Filed	No. Extra	Rate	Fee
TOTAL CLAIMS	65 - 20 =	45	x 18 =	$810.00
INDEPENDENT CLAIMS	19 - 3 =	16	x 80 =	$1,280.00
[ ] MULTIPLE DEPENDENT CLAIMS PRESENTED				$0.00
BASIC FEE				$710.00
TOTAL				$2,800.00

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes et al.	Examiner: Unknown
Serial No.:	Unknown	Group Art Unit: Unknown
Filed:	Herewith	Docket: 303.324US4
Title:	TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE	

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

When the above-identified patent application is taken up for consideration, please amend the application as follows:

IN THE SPECIFICATION

On page 1, line 5, before "**Field of the Invention**", please insert the sentence, --This application is a continuation of U.S. Serial No. 08/903,452, filed on July 29, 1997.--

IN THE CLAIMS

Please cancel claims 1-35 without prejudice and add the following new claims 36-100.

36. A transistor comprising:

a source region, a drain region, a channel region between the source and drain regions, and a gate separated from the channel region by an insulator, the gate formed of a silicon carbide compound $Si_{1-x}C_x$, wherein x is greater than 0.5 to establish a desired value of a barrier energy between the gate and the insulator.

37. A transistor comprising:

a source region, a drain region, a channel region between the source and drain regions, and a gate separated from the channel region by an insulator, the gate formed of a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a predetermined value approximately between 0.5 and 1.0 to establish a desired value of a barrier energy between the gate and the insulator.

38. The transistor of claim 36, wherein the value of the barrier energy is approximately between 0 eV and 2.8 eV.

39. The transistor of claim 36, wherein the insulator is formed of silicon dioxide.

40. A transistor comprising:

a source region, a drain region, a channel region between the source and drain regions, and an electrically isolated floating gate separated from the channel region by an insulator, the floating gate formed of a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a predetermined value approximately between 0 and 1.0 to establish a desired value of a barrier energy between the gate and the insulator: and

a control gate, separated from the floating gate by an intergate dielectric.

41. The transistor of claim 40, wherein the intergate dielectric is formed of silicon dioxide.

42. The transistor of claim 40, wherein the predetermined value x is selected to provide a desired charge retention time of the floating gate.

43. The transistor of claim 40, wherein the predetermined value x is selected to provide a desired range of photon wavelengths most likely to be absorbed by the floating gate whereby electrons are emitted from the floating gate in response to the absorbed photons.

44. The transistor of claim 43, wherein the emission of electrons from the floating gate in response to incident photons changes a current conductance between the source and drain regions.

45. The transistor of claim 36, wherein the gate is formed of a material selected from the group consisting of monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

46. A device for detecting light, the device comprising:

a source region;

a drain region;

a channel region between the source and drain regions; and

a floating gate separated from the channel region by an insulator, the floating gate formed of a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a predetermined value approximately between 0 and 1.0 to establish a desired value of a barrier energy between the floating gate and the insulator for charge storage upon the floating gate and emission of charge from the floating gate in response to absorbed incident photons.

47. The device of claim 46, further comprising a control gate located adjacent to the floating gate and separated therefrom by an interlayer dielectric.

48. The device of claim 46, wherein x is selected at a predetermined value that is approximately between 0.5 and 1.0.

49. The device of claim 46, wherein x is selected at a predetermined value to provide a desired value of the barrier energy that is approximately between 0 eV and 2.8 eV.

50. The device of claim 46, wherein the predetermined value x is selected to provide a desired range of photon wavelengths most likely to be absorbed by the floating gate whereby electrons are emitted from the floating gate in response to the absorbed photons.

51. The device of claim 46, wherein the emission of charge from the floating gate in response to incident photons changes a current conductance between the source and drain regions.

52. A memory device comprising:

a plurality of memory cells, wherein each memory cell includes a transistor comprising:

a source region;

a drain region;

a channel region between the source and drain regions;

a floating gate separated from the channel region by an insulator, the

floating gate formed of a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a predetermined value approximately between 0 and 1.0 to establish a desired value of a barrier energy between the gate and the insulator; and

a control gate located adjacent to the floating gate and separated therefrom by an interlayer dielectric.

53. The device of claim 52, wherein the value of x is selected approximately between 0.5 and 1.0.

54. The device of claim 52, wherein the value of the barrier energy is approximately between 0 eV and 2.8 eV.

55. The device of claim 52, wherein the value of x is selected to provide a desired charge retention time of the floating gate.

56. A transistor comprising:

a source region formed in a silicon substrate;

a drain region formed in the silicon substrate;

a channel region in the silicon substrate between the source region and the drain region; and

a gate separated from the channel region by an insulator, the gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be between 0 and 1.0.

57. The transistor of claim 56 wherein:

the silicon substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region formed in the silicon substrate;

the drain region comprises an n+-type drain region formed in the silicon substrate; and

the insulator comprises a layer of silicon dioxide.

58. The transistor of claim 56 wherein the gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

59. A transistor comprising:

a source region formed in a substrate;

a drain region formed in the substrate;

a channel region in the substrate between the source region and the drain region; and

a gate separated from the channel region by an insulator, the gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be between 0.5 and 1.0.

60. The transistor of claim 59 wherein:

the substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region formed in the substrate;

the drain region comprises an n+-type drain region formed in the substrate; and

the insulator comprises a layer of silicon dioxide.

61. The transistor of claim 59 wherein the gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

62. A transistor comprising:

a source region formed in a substrate;

a drain region formed in the substrate;

a channel region in the substrate between the source region and the drain region; and

a gate separated from the channel region by an insulator, the gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be between 0.1 and 0.5.

63. The transistor of claim 62 wherein:

the substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region formed in the substrate;

the drain region comprises an n+-type drain region formed in the substrate; and

the insulator comprises a layer of silicon dioxide.

64. The transistor of claim 62 wherein the gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

65. A transistor comprising:

a source region formed in a substrate;

a drain region formed in the substrate;

a channel region in the substrate between the source region and the drain region; and

a gate separated from the channel region by an insulator, the gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be less than 0.5.

66. The transistor of claim 65 wherein:

the substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region formed in the substrate;

the drain region comprises an n+-type drain region formed in the substrate; and

the insulator comprises a layer of silicon dioxide.

67. The transistor of claim 65 wherein the gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

68. A floating gate transistor comprising:

a source region formed in a silicon substrate;

a drain region formed in the silicon substrate;

a channel region in the silicon substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be between 0 and 1.0; and

a control gate separated from the floating gate by an intergate dielectric.

69. The floating gate transistor of claim 68 wherein:

the silicon substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region formed in the silicon substrate;

the drain region comprises an n+-type drain region formed in the silicon substrate;

the insulator comprises silicon dioxide; and

the intergate dielectric comprises silicon dioxide.

70. The floating gate transistor of claim 68 wherein the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

71. A floating gate transistor comprising:

a source region formed in a substrate;

a drain region formed in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be between 0.5 and 1.0; and

a control gate separated from the floating gate by an intergate dielectric.

72. The floating gate transistor of claim 71 wherein:
the substrate comprises a p-type silicon substrate;
the source region comprises an n+-type source region formed in the substrate;
the drain region comprises an n+-type drain region formed in the substrate;
the insulator comprises silicon dioxide; and
the intergate dielectric comprises silicon dioxide.

73. The floating gate transistor of claim 71 wherein the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

74. A floating gate transistor comprising:
a source region formed in a substrate;
a drain region formed in the substrate;
a channel region in the substrate between the source region and the drain region;
a floating gate separated from the channel region by an insulator, the floating gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be between 0.1 and 0.5; and
a control gate separated from the floating gate by an intergate dielectric.

75. The floating gate transistor of claim 74 wherein:
the substrate comprises a p-type silicon substrate;
the source region comprises an n+-type source region formed in the substrate;
the drain region comprises an n+-type drain region formed in the substrate;
the insulator comprises silicon dioxide; and
the intergate dielectric comprises silicon dioxide.

76. The floating gate transistor of claim 74 wherein the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a

polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

77. A floating gate transistor comprising:

a source region formed in a substrate;

a drain region formed in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be to be less than 0.5; and

a control gate separated from the floating gate by an intergate dielectric.

78. The floating gate transistor of claim 77 wherein:

the substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region formed in the substrate;

the drain region comprises an n+-type drain region formed in the substrate;

the insulator comprises silicon dioxide; and

the intergate dielectric comprises silicon dioxide.

79. The floating gate transistor of claim 77 wherein the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

80. A floating gate transistor comprising:

a source region formed in a substrate;

a drain region formed in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be between 0.5 and 0.75; and

a control gate separated from the floating gate by an intergate dielectric.

81. The floating gate transistor of claim 80 wherein:
the substrate comprises a p-type silicon substrate;
the source region comprises an n+-type source region formed in the substrate;
the drain region comprises an n+-type drain region formed in the substrate;
the insulator comprises silicon dioxide; and
the intergate dielectric comprises silicon dioxide.

82. The floating gate transistor of claim 80 wherein the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

83. A floating gate transistor comprising:
a source region formed in a substrate;
a drain region formed in the substrate;
a channel region in the substrate between the source region and the drain region;
a floating gate separated from the channel region by an insulator, the floating gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be between 0.75 and 1.0; and
a control gate separated from the floating gate by an intergate dielectric.

84. The floating gate transistor of claim 83 wherein:
the substrate comprises a p-type silicon substrate;
the source region comprises an n+-type source region formed in the substrate;
the drain region comprises an n+-type drain region formed in the substrate;
the insulator comprises silicon dioxide; and
the intergate dielectric comprises silicon dioxide.

85. The floating gate transistor of claim 83 wherein the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

86. A system comprising:

a processor; and

a memory device coupled to the processor through a plurality of lines, the memory device comprising:

a control circuit; and

an array of floating gate transistor memory cells, each memory cell comprising:

a source region formed in a silicon substrate;

a drain region formed in the silicon substrate;

a channel region in the silicon substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be between 0 and 1.0; and

a control gate separated from the floating gate by an intergate dielectric.

87. The system of claim 86 wherein:

the silicon substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region formed in the silicon substrate;

the drain region comprises an n+-type drain region formed in the silicon substrate;

the insulator comprises silicon dioxide;

the intergate dielectric comprises silicon dioxide;

the lines comprise control lines, data lines, and address lines; and

the memory device further comprises a row decoder, a column decoder, and a voltage control circuit.

88. The system of claim 86 wherein the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

89. A system comprising:

a processor; and

a memory device coupled to the processor through a plurality of lines, the memory device comprising:

a control circuit; and

an array of floating gate transistor memory cells, each memory cell comprising:

a source region formed in a substrate;

a drain region formed in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be between 0.5 and 1.0; and

a control gate separated from the floating gate by an intergate dielectric.

90. The system of claim 89 wherein:

the substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region formed in the substrate;

the drain region comprises an n+-type drain region formed in the substrate;

the insulator comprises silicon dioxide;

the intergate dielectric comprises silicon dioxide;

the lines comprise control lines, data lines, and address lines; and

the memory device further comprises a row decoder, a column decoder, and a voltage control circuit.

91. The system of claim 89 wherein the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

92. A system comprising:

a processor; and

a memory device coupled to the processor through a plurality of lines, the memory device comprising:

a control circuit; and

an array of floating gate transistor memory cells, each memory cell comprising:

a source region formed in a substrate;

a drain region formed in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be between 0.5 and 0.75; and

a control gate separated from the floating gate by an intergate dielectric.

93. The system of claim 92 wherein:

the substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region formed in the substrate;

the drain region comprises an n+-type drain region formed in the substrate;

the insulator comprises silicon dioxide;

the intergate dielectric comprises silicon dioxide;

the lines comprise control lines, data lines, and address lines; and

the memory device further comprises a row decoder, a column decoder, and a voltage control circuit.

94. The system of claim 92 wherein the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

95. A system comprising:

a processor; and

a memory device coupled to the processor through a plurality of lines, the memory device comprising:

a control circuit; and

an array of floating gate transistor memory cells, each memory cell comprising:

a source region formed in a substrate;

a drain region formed in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, the floating gate comprising a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected to be between 0.75 and 1.0; and

a control gate separated from the floating gate by an intergate dielectric.

96. The system of claim 95 wherein:

the substrate comprises a p-type silicon substrate;

the source region comprises an n+-type source region formed in the substrate;

the drain region comprises an n+-type drain region formed in the substrate;

the insulator comprises silicon dioxide;

the intergate dielectric comprises silicon dioxide;

the lines comprise control lines, data lines, and address lines; and

the memory device further comprises a row decoder, a column decoder, and a voltage control circuit.

97. The system of claim 95 wherein the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

98. The transistor of claim 36, wherein the gate is an electrically isolated floating gate and further comprising a control gate, separated from the floating gate by an intergate dielectric comprising silicon dioxide.

99. The transistor of claim 37 wherein:

the insulator comprises silicon dioxide; and

the gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

100. The transistor of claim 40 wherein:

the insulator comprises silicon dioxide; and

the floating gate comprises a material selected from the group consisting of a monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

REMARKS

The original claims 1-35 have been canceled without prejudice, and new claims 36-100 have been added.

The applicant notes that U.S. Patent No. 5,801,401 to Forbes has been used as a reference in support of rejection under 35 U.S.C. § 103(a) in the parent U.S. Application Serial No. 08/903,452, filed on July 29, 1997, and from which priority is claimed. Forbes issued on September 1, 1998, which is after the July 29, 1997 filing date of the prior U.S. Application Serial Number 08/903,452, which is relied upon for an earlier filing date under 35 U.S.C. §120, as is listed above in the amendment to the specification. The Examiner therefore applied Forbes as prior art only under 35 U.S.C. § 102(e). The applicant does not admit that Forbes is prior art

and reserves the right to swear behind Forbes at a future date. The applicant also respectfully submits that Forbes is not prior art for the following reason.

As provided in Pub. Law 106-113, enacted November 29, 1999, a reference qualifying only under 35 U.S.C. § 102(e) cannot be used in support of a rejection under 35 U.S.C. § 103 where the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. *See*, 35 U.S.C. § 103(c). The applicant respectfully submits that the subject matter of Forbes and the present application were owned by the same person or subject to an obligation of assignment to the same person at the time the invention was made. Accordingly, Forbes cannot be used in support of rejection of the present claims under 35 U.S.C. § 103(a).

The applicant respectfully submits that all of the pending claims are in condition for allowance and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application.

CONCLUSION

The Applicant respectfully requests that the preliminary amendment described herein be entered into the record prior to examination and consideration of the above-identified application. Please charge any additional fees deemed necessary to Deposit Account 19-0743.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

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Date 18 OCTOBER 2000 By _____

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"Express Mail" mailing label number: EL618477137US
Date of Deposit: October 18, 2000
This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.

Attorney Docket No. 00303.324US1

TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE

Field of the Invention

The present invention relates generally to integrated circuit technology, and particularly to a silicon carbide gate transistor, such as a floating gate transistor, and complementary metal-oxide-semiconductor (CMOS) compatible methods of fabrication, and methods of use in memory and light detection devices.

Background of the Invention

Field-effect transistors (FETs) are typically produced using a standard complementary metal-oxide-semiconductor (CMOS) integrated circuit fabrication process. Such a process allows a high degree of integration for obtaining high circuit density with relatively few processing steps. Resulting FETs typically have gate electrodes composed of n-type conductively doped polycrystalline silicon (polysilicon) material.

The intrinsic properties of the polysilicon gate material affects operating characteristics of the FET. Silicon (monocrystalline and polycrystalline) has intrinsic properties that include a relatively small energy bandgap (E_g), e.g. approximately 1.2 eV, and a corresponding electron affinity (χ) that is relatively large, e.g. $\chi \approx 4.2$ eV. For example, for p-channel FETs fabricated by a typical CMOS process, these and other material properties result in a large turn-on threshold voltage (V_T) magnitude. As a result, the V_T magnitude must be downwardly adjusted by doping the channel region that underlies the gate electrode of the FET.

Conventional polysilicon gate FETs also have drawbacks that arise during use as a nonvolatile storage devices, such as in electrically erasable and programmable read only memories (EEPROMs). EEPROM memory cells typically use FETs having an

electrically isolated (floating) gate that affects conduction between source and drain regions of the FET. A gate dielectric is interposed between the floating gate and an underlying channel region between source and drain regions. A control gate is provided adjacent to the floating gate, separated therefrom by an intergate dielectric.

In such memory cells, data is represented by charge stored on the polysilicon floating gates. Fowler-Nordheim tunneling is one method that is used to store charge on the polysilicon floating gates during a write operation and to remove charge from the polysilicon floating gate during an erase operation. However, the relatively large electron affinity of the polysilicon floating gate presents a relatively large tunneling barrier energy at its interface with the underlying gate dielectric. The large tunneling barrier energy provides longer data retention times than realistically needed. For example, a data charge retention time at 85° C is estimated to be in millions of years for some floating gate memory devices. The large tunneling barrier also increases the time needed to store charge on the polysilicon floating gates during the write operation and the time needed to remove charge from the polysilicon floating gate during the erase operation. This is particularly problematic for "flash" EEPROMs, which have an architecture that allows the simultaneous erasure of many floating gate transistor memory cells. Since more charge must be removed from the many floating gates in a flash EEPROM, even longer erasure times are needed to accomplish this simultaneous erasure. There is a need in the art to obtain floating gate transistors allowing faster storage and erasure, such as millisecond erasure periods in flash EEPROMs.

Other problems result from the large erasure voltages that are typically applied to a control gate of the floating gate transistor in order to remove charge from the floating gate. These large erasure voltages are a consequence of the large tunneling barrier energy between the polysilicon floating gate and the underlying gate dielectric. The large erasure voltages can result in hole injection into the gate dielectric. This can cause erratic overerasure, damage to the gate dielectric, and introduction of trapping states in the gate dielectric. The high electric fields that result from the large erasure voltages can also result in reliability problems, leading to device failure. There is a

need in the art to obtain floating gate transistors that allow the use of lower erasure voltages. There is a need in the art for floating gate transistors capable of operating at lower programming and erasure voltages and having improved reliability.

Halvis et al. (U.S. Patent Number 5,369,040) discloses a charge-coupled device (CCD) photodetector which has transparent gate MOS imaging transistors fabricated from polysilicon with the addition of up to 50% carbon, and preferably about 10% carbon, which makes the gate material more transparent to the visible portion of the energy spectrum. The Halvis et al. patent is one example of a class of conventional CCD photodetectors that are directed to improving gate transmissivity to allow a greater portion of incident light in the visible spectrum to penetrate through the gate for absorption in the semiconductor substrate. However, the absorption of photons in the semiconductor substrate is limited to high energy photons exceeding a bandgap energy of the semiconductor substrate. There is a need in the art to detect lower energy photons independently of the semiconductor bandgap energy limitation. For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, the above described needs are unresolved in the art of fabrication of light detection devices, FETs, and EEPROMs using CMOS processes.

Summary of the Invention

The present invention includes a transistor having a gate formed of a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a predetermined value approximately between 0 and 1.0 to establish a desired value of a barrier energy between the gate and an adjacent insulator. The SiC gate is either electrically isolated (floating) or interconnected. In one embodiment, the gate is an electrically isolated floating gate, and the transistor further includes a control gate, separated from the floating gate by an intergate dielectric.

Another aspect of the invention provides a method of producing a transistor on a semiconductor substrate. Source and drain regions are formed, thereby defining a

channel region between the source and drain regions. An insulating layer is formed on the channel region. A gate is formed on the insulating layer. The gate comprises a silicon carbide compound $Si_{1-x}C_x$. The SiC composition x is selected at a predetermined value approximately between 0 and 1.0. In one embodiment, the value of the SiC composition x is selected to establish the value of a barrier energy between the gate and the insulator.

Another aspect of the invention provides light detection. Charge is stored on a floating gate of a transistor. Incident light is received at the floating gate, thereby removing at least a portion of the stored charge from the floating gate by the photoelectric effect. A change in conductance between the transistor source and drain is detected. In one embodiment, the method of detecting light includes selecting at least one wavelength of the incident light to which the floating gate transistor is most sensitive. In another light detecting embodiment, the invention provides a transistor that includes a floating gate separated from a channel region by an insulator. The floating gate is formed of a silicon carbide compound $Si_{1-x}C_x$. The SiC composition variable x is selected at a predetermined value approximately between 0 and 1.0 to establish the wavelength of incident light absorption to which the floating gate is sensitive. Charge is stored on the floating gate. Incident light is received at the floating gate, thereby removing at least a portion of the stored charge from the floating gate by the photoelectric effect. A change in conductance between the transistor source and drain is detected. Unlike conventional photodetectors, light is absorbed in the floating gate, thereby ejecting previously stored electrons therefrom. Also unlike conventional photodetectors, the light detector according to the present invention is actually more sensitive to lower energy photons as the semiconductor bandgap is increased.

In another embodiment, the transistor is used in a memory device that includes a plurality of memory cells. Each memory cell includes a transistor having a floating gate separated from the channel region by an insulator. The floating gate is formed of a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a predetermined value

approximately between 0 and 1.0 to establish a desired value of a barrier energy between the gate and the insulator.

In a flash electrically erasable and programmable read only memory (EEPROM) application, the SiC composition x is selected to provide the desired programming and erase voltage and time or data charge retention time. The lower barrier energy and increased tunneling probability of the SiC gate advantageously provides faster programming and erasure times for floating SiC gate transistors in flash EEPROM memories. This is particularly advantageous for "flash" EEPROMs in which many floating gate transistor memory cells must be erased simultaneously. Writing and erasure voltages are also advantageously reduced, minimizing the need for complicated and noisy on-chip charge pump circuits to generate the large erasure voltage. Lower erasure voltages also reduce hole injection into the gate dielectric that can cause erratic overerasure, damage to the gate dielectric, and introduction of trapping states in the gate dielectric. Reducing the erasure voltage also lowers the electric fields, minimizing reliability problems that can lead to device failure, and better accommodating downward scaling of device dimensions. Data charge retention time is decreased. Since conventional data charge retention times are longer than what is realistically needed, a shorter data charge retention time can be accommodated in order to obtain the benefits of a smaller barrier energy. The data charge retention time can be selected between seconds and millions of years by selecting the value of the SiC composition x, such as to obtain different memory functionality.

Brief Description of the Drawings

In the drawings, like numerals describe substantially similar components throughout the several views.

Figure **1** is a cross-sectional view illustrating generally one embodiment of a FET provided by the invention, which includes an electrically isolated (floating) or interconnected gate including a silicon carbide (SiC) compound.

Figure **2** is a graph illustrating generally barrier energy versus tunneling distance for SiC and conventional polysilicon gates.

Figures **3A**, **3B**, and **3C** illustrate generally electron affinities of various SiC compositions and of silicon dioxide, and the resulting interfacial barrier energy therebetween.

Figure **4** is a cross-sectional view illustrating generally a variable electron affinity floating SiC gate field-effect transistor (FET) provided by the invention.

Figure **5** is a graph that illustrates generally the relationship between retention time and barrier energy, and also the relationship between erase time and barrier energy.

Figure **6** illustrates generally a flash EEPROM memory having memory cells that include an SiC gate transistor according to the present invention.

Figure **7** is a cross-sectional schematic diagram of the floating gate transistor that illustrates generally its application according to the present invention as a light detector or imaging device.

Figure **8** is a cross-sectional schematic diagram that illustrates generally how incident light is detected by the absorption of photons by the floating gate.

Figure **9** is a graph that illustrates generally, by way of example, the SiC absorption coefficient as a function of wavelength and photon energy.

Figure **10** is a graph illustrating generally barrier height versus tunneling distance, and further illustrating the absorption of light energy by the floating gate.

Figure **11** is a graph illustrating generally barrier height versus tunneling distance, and distinguishing photoelectric absorption of incident light in the SiC floating gate from valence-to-conduction band electron transitions.

Figures **12A**, **12B**, **12C**, **12D**, **12E**, **12F**, and **12G** illustrate generally examples of process steps for fabricating n-channel and p-channel SiC gate FETs according to the present invention, including the fabrication of SiC floating gate transistors.

Detailed Description of the Invention

In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. The embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural and electrical changes may be made without departing from the scope of the present invention. The terms wafer and substrate used in the following description include any semiconductor-based structure having an exposed surface with which to form the integrated circuit structure of the invention. Wafer and substrate are used interchangeably to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims.

The present invention includes a field-effect transistor (FET) having a gate that is formed of at least partially crystalline (e.g., monocrystalline, polycrystalline, microcrystalline, or nanocrystalline) diamond-like silicon carbide (SiC) material, which includes any material that incorporates both silicon and carbon into the gate region of a FET. The SiC gate FET includes characteristics such as, for example, a lower electron affinity than a conventional polycrystalline silicon (polysilicon) gate FET. Another aspect of the invention provides a tailored SiC material composition for use in conjunction with a particular gate dielectric, or for particular applications, such as data storage (memory) and imaging.

Figure **1** is a cross-sectional view illustrating generally, by way of example, one embodiment of a n-channel FET provided by the invention. The invention is

understood to also include a p-channel FET embodiment. The n-channel FET includes a source **102**, a drain **104**, and a gate **106**. A gate dielectric, such as thin oxide layer **118** or other suitable insulator, is interposed between gate **106** and substrate **108**. In one embodiment, source **102** and drain **104** are fabricated by forming highly doped (n+) regions in a lightly doped (p-) silicon semiconductor substrate **108**. In another embodiment, substrate **108** includes a thin semiconductor surface layer formed on an underlying insulating portion, such as in a semiconductor-on-insulator (SOI) or other thin film transistor technology. Source **102** and drain **104** are separated by a predetermined length in which a channel region **110** is formed.

According to one aspect of the invention, gate **106** is formed of silicon carbide (SiC) material, which includes any material that incorporates both silicon and carbon into gate **106**. The silicon carbide material forming gate **106** is described more generally as $Si_{1-x}C_x$, where x is a composition variable that defines the SiC material composition. According to another aspect of the invention, the SiC composition x is selected at a predetermined value that establishes the value of a barrier energy (also referred to as a barrier potential, potential barrier, tunneling barrier, interface barrier, or barrier) between gate **106** and thin oxide layer **118** (or other gate dielectric). For example, in one embodiment, the SiC composition is approximately stoichiometric, i.e., $x \approx 0.5$. However, other embodiments of the invention include less carbon (i.e., $x < 0.5$) or more carbon (i.e., $x > 0.5$). For example, but not by way of limitation, one embodiment of the SiC gate material is illustrated by $0.1 < x < 0.5$. Another example embodiment is illustrated by way of example, but not by way of limitation, by $0.4 < x < 0.6$. Still another embodiment is illustrated by way of example, but not by way of limitation, by $0.5 < x < 1.0$. As described below, the SiC composition x is selected as a predetermined value in order to tailor the barrier for particular applications. In one embodiment, the SiC composition x is uniform over a particular integrated circuit die. In another embodiment, the SiC composition x is differently selected at different locations on the integrated circuit die, such as by additional masking or processing steps, to obtain different device characteristics on the same integrated circuit die.

In one embodiment, an insulating layer, such as silicon dioxide (oxide) **114** or other insulating layer, is formed by chemical vapor deposition (CVD). Oxide **114** isolates gate **106** from other layers, such as layer **112**. In another embodiment, gate **106** is oxidized to form at least a portion of oxide **114** isolating gate **106** from other layers such as layer **112**. In one embodiment, for example, layer **112** is a polysilicon or other control gate in a floating gate transistor. According to techniques of the present invention, the floating gate transistor is used in an electrically erasable and programmable read-only memory (EEPROM) memory cell, such as a flash EEPROM, or in a floating gate transistor photodetector or imaging device, as described below. In these embodiments, gate **106** is floating (electrically isolated) for charge storage thereupon. The present invention offers considerable advantages to the known EEPROM techniques used for charge storage on floating gate **106**. In another embodiment, for example, layer **112** is a metal or other conductive interconnection line that is located above gate **106**.

The upper layers, such as layer **112** are covered with a layer **116** of a suitable insulating material in the conventional manner, such as for isolating and protecting the physical integrity of the underlying features. Gate **106** is isolated from channel **110** by an insulating layer such as thin oxide layer **118**, or any other suitable dielectric material. In one embodiment, thin oxide layer **118** is a gate oxide layer that can be approximately 100 angstroms (Å) thick, such as for conventional FET operation. In another embodiment, such as in a floating gate transistor, thin oxide layer **118** is a tunnel oxide material that can be approximately 50 - 100 Å thick.

The SiC gate **106** has particular advantages over polysilicon gates used in floating gate and conventional FETs fabricated using a conventional complementary metal-oxide-semiconductor (CMOS) process due to different characteristics of the SiC material. For example, stoichiometric SiC ($x \approx 0.5$) is a wide bandgap semiconductor material with a bandgap energy of about 2.1 eV, in contrast to silicon (monocrystalline or polycrystalline), which has a bandgap energy of about 1.2 eV. Stoichiometric SiC

has an electron affinity of about 3.7 to 3.8 eV, while silicon has an electron affinity of about 4.2 eV.

The smaller electron affinity of the SiC gate **106** material reduces the barrier energy at the interface between gate **106** and thin oxide layer **118**. In an embodiment in which thin oxide layer **118** is a tunnel oxide in a floating gate transistor EEPROM memory cell, the lower electron affinity of SiC reduces the tunneling distance and increases the tunneling probability. This speeds the write and erase operations of storing and removing charge to and from floating gate **106**. This is particularly advantageous for "flash" EEPROMs in which many floating gate transistor memory cells must be erased simultaneously. The large charge that must be transported by Fowler-Nordheim tunneling during the erasure of a flash EEPROM typically results in relatively long erasure times. By reducing the tunneling distance and increasing the tunneling probability, the SiC gate **106** reduces erasure times in flash EEPROMs.

According to one aspect of the present invention, the exact value of the SiC composition *x* is selected to obtain the desired barrier potential for the particular application. The predetermined value the SiC composition *x* establishes the particular electron affinity, χ, such as between that of stoichiometric SiC (about 3.7 to 3.8 eV) and a value $\chi < 0$ eV. As a result, the barrier energy is further decreased from that of stoichiometric SiC by the exact amount desired. This speeds storage and removal of charge to and from the floating gate **106** during write and erase operations.

Lowering the barrier potential also decreases the data charge retention time of the charge stored on the floating gate **106**. Conventional polysilicon floating gates have a data charge retention time estimated in the millions of years at a temperature of 85 degrees C. Since such long data charge retention times are longer than what is realistically needed, a shorter data charge retention time can be accommodated in order to obtain the benefits of a smaller barrier energy. According to one aspect of the present invention, the SiC composition *x* is selected to establish the particular data charge retention time. For example, the data charge retention time can be selected between seconds and millions of years.

Figure **1** illustrates generally, by way of example, a complementary metal-oxide-semiconductor (CMOS) compatible n-channel FET that includes an SiC gate **106**, which may be floating or electrically interconnected. In one embodiment, for example, the FET can be formed on substrate **108** using an n-well CMOS process for monolithic CMOS fabrication of n-channel and p-channel FETs on a common substrate. The invention includes both n-channel and p-channel FETs that have a polycrystalline or microcrystalline SiC gate **106**. Thus, with appropriate doping, the FET of Figure **1** can be a p-channel FET. The p-channel and n-channel SiC gate FETs are useful for any application in which conventionally formed polysilicon gate FETs are used, including both electrically driven and floating gate applications.

Figure **2** illustrates generally how the smaller SiC electron affinity provides a smaller barrier energy than a conventional polysilicon gate. The smaller SiC barrier energy reduces the energy to which the electrons must be excited to be stored on the SiC gate **106** by thermionic emission. The smaller barrier energy also reduces the distance that electrons stored on the gate have to traverse, such as by Fowler-Nordheim tunneling, to be stored upon or removed from the SiC gate **106**. The reduced tunneling distance allows easier charge transfer, such as during writing or erasing data in a floating gate transistor in a flash EEPROM memory cell. In Figure **2**, "do" represents the tunneling distance of a typical polysilicon floating gate transistor due to the barrier height represented by the dashed line "OLD". The tunneling distance "dn" corresponds to a SiC gate and its smaller barrier height represented by the dashed line "NEW". Even a small reduction in the tunneling distance results in a large increase in the tunneling probability, because the tunneling probability is an exponential function of the reciprocal of the tunneling distance. The increased tunneling probability of the SiC gate **106** advantageously provides faster programming and erasure times for floating SiC gate transistors in flash EEPROM memories. The smaller bandgap of floating SiC gate transistors have a smaller turn-on threshold voltage magnitude, thereby also allowing operation of such flash EEPROM memories at lower power supply voltages.

Figures **3A - 3C** illustrate generally by way of example, but not by way of limitation, different selections of the predetermined value of the SiC composition x. Differently selected values of the SiC composition x provide different resulting barrier energies at the interface between gate **106** and the adjacent thin oxide layer **118** (or other gate or tunneling dielectric). Figures **3A - 3C** illustrate, by way of example, but not by way of limitation, the use of a silicon dioxide gate insulator such as thin oxide layer **118**. However, the invention includes the use of any other gate insulator materials in combination with the SiC gate **106**.

In Figures **3A - 3C**, the electron affinities, χ, of each of the thin oxide layer **118** and SiC gate **106** are measured with respect to the vacuum level **300**. In the thin oxide layer **118**, the electron affinity, χ, is defined by the difference between the oxide conduction band **302** and the vacuum level **300**. In the SiC gate **106**, the electron affinity, χ, is defined by the difference between the semiconductor conduction band edge **305** and the vacuum level **300**. The barrier energy at the interface between thin oxide layer **118** and SiC gate **106** is illustrated by the difference between their respective electron affinities, χ.

In Figure **3A**, the SiC composition is selected at $x \approx 0$, which is an extreme limit in which the SiC gate **106** material composition is approximately pure silicon (e.g., polycrystalline or microcrystalline). As seen in Figure **3A**, the resulting electron affinity in the gate **106** material is $\chi \approx 4.2$ eV. The electron affinity in thin oxide layer **118** is $\chi \approx 0.9$ eV. The resulting barrier energy is approximately 3.3 eV. In a memory application using a floating gate **106**, the 3.3 eV barrier energy results in long data charge retention times (estimated in millions of years at a temperature of 85 degrees C) together with large erasure voltages and long write and erase times. In an imaging application using a floating gate **106**, the 3.3 eV barrier energy requires relatively high energy photons (i.e., high frequency and short wavelength) to eject stored electrons from the floating gate **106**.

In Figure **3B**, the SiC composition is selected at $x \approx 0.5$, for which the SiC gate **106** material is approximately stoichiometric SiC. As seen in Figure **3B**, the resulting

electron affinity in the gate **106** material is $\chi \approx 3.7$ eV. The electron affinity in thin oxide layer **118** is $\chi \approx 0.9$ eV. The resulting barrier energy is approximately 2.8 eV. In a memory application using a floating gate **106**, the 2.8 eV barrier energy results in shorter charge retention times than are obtained than in the case described with respect to Figure **3A**, together with smaller erasure voltages and shorter write and erase times. In an imaging application using a floating gate **106**, the 2.8 eV barrier energy needs less photon energy (i.e., lower frequency and longer wavelength) to eject electrons from the floating gate **106** than in the case described with respect to Figure **3A**.

In Figure **3C**, the SiC composition is selected at $x \approx 1$, which is an extreme limit in which the material is substantially pure carbon (i.e., diamond). As seen in Figure **3C**, the resulting electron affinity in the gate material is $\chi \approx -0.4$ eV. The electron affinity in the silicon dioxide insulator **118** is $\chi \approx 0.9$ eV. The resulting barrier energy is approximately -1.3 eV. In this case, electrons will not stay in the conduction band of the diamond gate **106** material, but will instead move into the thin oxide layer **118**.

Thus, the barrier energy at the interface between thin oxide layer **118** and SiC gate **106** is adjusted by tuning the SiC composition x. The SiC gate material compounds can be doped p-type or n-type, either during formation or by a subsequent doping step. However, the SiC films are quite conductive even when intrinsic. In floating gate applications, the SiC films need not be very conductive since they are not used for interconnection wiring. An SiC floating gate **106** need only allow for redistribution of carriers in the floating gate **106**. Microcrystalline SiC compounds have a smaller electron affinity than polycrystalline SiC compounds. In one embodiment of the present invention, the barrier potential is adjusted by selecting between microcrystalline and polycrystalline SiC compounds for the gate **106** material.

Floating Gate Memory Device

Figure **4** is a cross-sectional view of a transistor, similar to that of Figure **1**, illustrating generally a floating gate transistor embodiment of the invention, such as for

use as a nonvolatile memory cell in a flash EEPROM. In one embodiment, floating gate **106** is a polycrystalline or microcrystalline SiC compound for which $0.5 < x < 1.0$.

By using polycrystalline or microcrystalline SiC for floating gate **106**, a lower barrier energy is obtained at the interface between gate **106** and thin oxide layer **118**. The exact barrier energy is established by selecting the predetermined value of the SiC composition x. The lower barrier energy provides a larger tunneling probability during write and erase operations. Write and erasure voltages and times are reduced. Secondary problems that are normally associated with erasure of charge stored on polysilicon gates, such as electron trap creation and hole injection, are correspondingly reduced along with the erasure voltage.

In one embodiment, the exact value of the SiC composition x is selected to establish a barrier energy that is large enough to prevent electrons from being thermally excited over the barrier at high operating temperatures, such as at a temperature of 85° C, as this could allow the stored data charges to leak from the floating gate over a long period of time. The high barrier energy of a polysilicon floating gate material provides a longer than realistically needed data charge retention time that is estimated in millions of years. The SiC composition x is selected to obtain a lower barrier energy, providing data retention times that are more suited to the particular application. In one embodiment of the present invention, the SiC composition x is selected to obtain typical data charge retention times between seconds and millions of years.

In one embodiment, the invention includes operation of a SiC floating gate transistor memory device. Floating gate **106** can be programmed, by way of example, but not by way of limitation, by providing about 12 volts to control gate **112**, and providing about 6 volts to drain **104**, and providing about 0 volts to source **102**. This creates an inversion layer in channel region **110**, in which electrons are accelerated from source **102** toward drain **104**, acquiring substantial kinetic energy. High energy "hot electrons' are injected through thin oxide layer **118** onto the polycrystalline or microcrystalline SiC floating gate **106**. Floating gate **106** accumulates the hot electrons as stored data charges.

The change in the charge stored on floating gate **106** changes the threshold voltage of the n-channel floating gate FET of Figure **4**. When control gate **112** is driven to a read voltage during a read operation, the change in charge stored on floating gate **106** results in a change in current between drain **104** and source **102**. Thus, detection of the change in charge stored on floating gate **106** by sensing drain-source current conductance advantageously uses the appreciable transconductance gain of the floating gate FET of Figure **4**. Either analog or digital data can be stored as charge on floating gate **106** and read back as a conductance between drain region **104** and source region **102**.

The erase time for the memory cell is determined by the height of the barrier between floating gate **106** and thin oxide layer **118**. A lower barrier energy results in a shorter tunneling distance, as described with respect to Figure **2**. This, in turn, results in a faster erase operation, lower erasure voltages, or both faster erase operation and lower erasure voltages. Short erase times are normally particularly desirable in flash memories, in which many memory cells must be simultaneously erased. However, a lower barrier energy also means a shorter data charge retention time due to thermal excitation of electrons over or tunneling of electrons through the barrier.

According to the invention, the barrier energy is varied by changing the SiC composition x. By selecting the predetermined value of the SiC composition x, the data charge retention time can be established at a value that is, for example, between seconds and millions of years. By changing the SiC composition x, a flash memory device that incorporates the SiC floating gate transistor provides a data charge retention time that is tailored to the particular application.

For example, by setting the SiC composition at about $0.75 < x < 1.0$, the flash memory device can be made to emulate a dynamic random access memory (DRAM), with data charge retention times on the order of seconds. On the other hand, for example, by setting the SiC composition at about $0.5 < x < 0.75$, the flash memory device can be made to emulate a hard disk drive, by providing a data charge retention time on the order of years. According to one aspect of the present invention, one

memory device provides different memory functions by selecting the SiC composition x. In one embodiment, floating gate transistors having different SiC compositions x are provided on the same integrated circuit, thereby providing differently functioning memory cells on the same integrated circuit.

Figure **5** is a conceptual diagram, using rough order of magnitude estimates, that illustrates generally how erase and retention times vary with the barrier energy for a particular value of erasure voltage at a particular temperature of 85° C. The probability of thermal excitation and emission over or tunneling through the barrier is an exponential function of the barrier energy. A lower barrier provides exponentially shorter erase and retention times. The particular memory application requirements determine the needed memory retention time, whether seconds or years. From this memory retention time, the barrier energy required and the erase time for a particular voltage can be determined using an engineering graph similar to that of Figure **5**. Thus, the SiC composition x is selected to provide a retention time on the order of seconds or years, depending upon the function required for the memory device. According to one aspect of the present invention, for example, the memory device can emulate or replace DRAMs or hard disk drives by selecting the SiC composition x to establish the appropriate data charge retention time.

Figure **6** is a simplified block diagram illustrating generally one embodiment of a memory **600** system, according to one aspect of the present invention, in which SiC gate FETs are incorporated. In one embodiment, memory **600** is a flash EEPROM, and the SiC gate FETs are floating gate transistors that are used for nonvolatile storage of data as charge on the SiC floating gates. However, the SiC gate FETs can have electrically interconnected gates, and can be used in other types of memory systems, including SDRAM, SLDRAM and RDRAM devices, or in programmable logic arrays (PLAs), or in any other application in which transistors are used.

Figure **6** illustrates, by way of example, but not by way of limitation, a flash EEPROM memory **600** comprising a memory array **602** of multiple memory cells. Row decoder **604** and column decoder **606** decode addresses provided on address lines

608 to access addressed SiC gate floating gate transistors in the memory cells in memory array 602. Command and control circuitry 610 controls the operation of memory 600 in response to control signals received on control lines 616 from a processor 601 or other memory controller during read, write, and erase operations. Voltage control 614 is provided to apply appropriate voltages to the memory cells during programming and erasing operations. It will be appreciated by those skilled in the art that the memory of Figure 6 has been simplified for the purpose of illustrating the present invention and is not intended to be a complete description of a flash EEPROM memory.

Floating Gate Imaging Device

According to another aspect of the present invention, the SiC floating gate transistor of Figure 4 is used in light detection applications, such as a photodetector or imaging device. In this embodiment of the invention, light is detected by the absorption of photons by the SiC floating gate 106. This is distinguishable from other types of imaging devices, such as sensors using a charge-coupled device (CCD) or a photodiode detector, in which light is absorbed in the semiconductor substrate, thereby producing charge carriers that are detected.

According to one embodiment of the present invention, charge is stored on the SiC floating gate 106, such as by known EEPROM charge storage techniques. The imaging device is exposed to incident light. Incident photons having enough energy to eject an electron by photoelectric emission from floating gate 106 are detected by a resulting change in drain-source conductance of the imaging device. Thus, the light detector of the present invention advantageously utilizes the transconductance gain of the floating gate transistor. In one embodiment of the invention, the wavelength to which the light detector is sensitive is established by selecting the SiC composition x of floating gate 106.

Figure 7 is a cross-sectional schematic diagram of the floating gate transistor that illustrates generally its application according to the present invention as a light

detector or imaging device. In Figure 7, floating gate **106** is charged by the injection of hot electrons **700** through thin oxide layer **118** under the SiC floating gate **106**. This change in charge on floating gate **106** changes the threshold voltage of the n-channel floating gate FET. As a result, when control gate **112** is driven to a read voltage during a read operation, a large change in drain-source current is obtained through the transconductance gain of the floating gate transistor.

Figure **8** is a cross-sectional schematic diagram that illustrates generally how incident light **800** is detected by the absorption of photons by floating gate **106**. The photons must have enough energy to cause electrons **700** stored on floating gate **106** to overcome the barrier at the interface between floating gate **106** and thin oxide layer **118** and be ejected from floating gate **106** back into the semiconductor or SOI substrate by the photoelectric effect. A small electric field in thin oxide layer **118**, such as results from the presence of electrons **700** stored on floating gate **106**, assists in ejecting the electrons **700** toward substrate **108**. Detection or imaging of visible wavelengths of incident light **800** requires a low electron affinity floating gate **106**. The present invention allows the electron affinity of floating gate **106** to be tailored by selecting the particular value of the SiC composition of floating gate **106**.

Figure **9** is a graph that illustrates generally, by way of example, the SiC absorption coefficient as a function of wavelength and photon energy. Several values of the SiC composition x are illustrated, where $0 < x < 1.0$. For example, by setting the SiC composition $x \approx 0.5$ (i.e., approximately stoichiometric SiC), the resulting light absorption is illustrated generally by line **910**. In another example, by setting the SiC composition $x \approx 0$ (i.e., approximately pure polycrystalline or microcrystalline Si), the resulting light absorption is illustrated generally by line **912**. In yet another example, by setting the SiC composition described approximately by $0.5 < x < 1.0$, the resulting light absorption is illustrated generally by line **914**.

Figure **10** further illustrates the absorption of light energy by floating gate **106**. In Figure **10**, the incident photons have sufficient energy to allow electrons **700** stored on floating gate **106** to overcome the "new" barrier **1000** such that they are emitted from

floating gate **106** back toward the semiconductor or SOI substrate **108**, thereby discharging floating gate **106**. "Old" barrier **1005**, which represents a Si-SiO_2 interface, is higher than "new" barrier **1000** of the SiC-SiO_2 interface. As a result, a light detector having an SiC floating gate **106** is sensitive to lower energy photons than a light detector having an Si floating gate.

In one embodiment, SiC floating gate **106** is doped n-type to maximize the number of conduction band electrons **700** in floating gate **106** and the absorption of incident light. Visible light has a photon energy of about 2 eV. For detection of visible light, the barrier energy at the interface between floating gate **106** and thin oxide layer **118** should be less than or equal to about 2 eV. However, most common gate materials have larger barrier energies with an adjacent silicon dioxide insulator. For example, a conventional polysilicon floating gate **106** results in a barrier energy of about 3.3 eV.

According to one aspect of the present invention, polycrystalline or microcrystalline SiC is used as the material for floating gate **106**. The SiC composition x is selected for sensitivity to particular wavelengths of light, and the barrier energy is established accordingly. For example, in one embodiment, the SiC composition x is selected in the range $0.5 < x < 1.0$ such that barrier energy is less than or equal to about 2 eV. As a result, the floating gate transistor light detector is sensitive to visible light. According to another aspect of the invention, the floating gate transistor light detector is made sensitive to different portions of the light spectrum by adjusting the barrier energy through the selection of the SiC composition x. The SiC composition x can also be different for different floating gate transistors on the same integrated circuit in order to yield different sensitivities to different wavelengths of light.

Figure **11** illustrates generally how the above-described photoelectric absorption of incident light in the SiC floating gate **106** is distinguishable from, and independent of, valence-to-conduction band electron transitions, which is the common photon absorption mechanism of most diode or CCD photodetectors or imaging devices. Conventional photon absorption is illustrated by the band-to-band electron energy transition **1100**. Photon absorption according to the present invention is illustrated by

the emission **1105** of a conduction band electron **700** from floating gate **106** over the barrier **1000** between the floating gate semiconductor conduction band **1110** and oxide conduction band **1115**.

The semiconductor bandgap is defined by the energy difference between semiconductor conduction band **1110** and semiconductor valence band **1120**. Exciting an electron from the valence band **1120** low energy state to a conduction band **1110** high energy state requires absorption of an incident photon of energy exceeding the bandgap of the semiconductor material. For diamond-like SiC compounds, these band-to-band transitions occur only at very high photon energies, such as for ultraviolet light. By contrast, photoelectric emission **1105** of electrons from floating gate **106** only requires that the incident photon energy exceed the barrier **1000** between floating gate **106** and thin oxide layer **118**. Since the present invention allows the barrier **1000** energy to be less than the 2 eV energy of a visible photon by an appropriate selection of the SiC composition x, and even allows a negative barrier **1000** energy, a wide spectrum of light detection is obtained.

In conventional photodetectors, only high energy photons are detected as the bandgap is increased (i.e., as the bandgap becomes larger, first red, then blue, and finally ultraviolet light is required for band-to-band photon absorption). According to the present invention, a larger bandgap typically results in a smaller barrier **1000** energy, thereby allowing detection of even lower energy photons as the bandgap is increased (i.e., as the bandgap becomes larger, the detector becomes sensitive not only to ultraviolet, but to blue, then red, and finally to infrared wavelengths). As a result, the present invention can be used for visible and infrared light detection and imaging, including camera-like operations, and can employ lenses, shutters, or other such known imaging techniques.

Figure **11** illustrates generally, by way of example, but not by way of limitation, the absorption of red light with photon energies of around 2 eV in the SiC floating gate **106**. In one embodiment, the SiC composition x is selected such that the barrier **1000** energy between SiC floating gate **106** and thin oxide layer **118** is less than (or much less

than) 2 eV, while the bandgap for the SiC floating gate **106** is much higher than 2 eV. In this embodiment, incident photons generate negligible electron-hole pairs or valence-to-conduction band transitions in floating gate **106**. Instead, absorption of photons is substantially entirely the result of photoelectric emission of electrons from floating gate **106**. While the quantum efficiency associated with the photoelectric effect can be low (e.g., less than one electron emitted per one hundred photons) the floating gate transistor offers appreciable transconductance gain. Emitting a single electron from the floating gate changes the number of electrons flowing out of the drain **104** by thousands. By adjusting the SiC composition *x* of floating gate **106**, the floating gate detector device is adjusted for optimum response over almost the entire optical spectrum, from infrared through visible light to ultraviolet. In a further embodiment of the invention, sensitivity is improved by doping the SiC floating gate **106** n-type, to increase the number of conduction band electrons stored on floating gate **106**.

Process

Figures **12A** - **12G** illustrate generally examples of CMOS-compatible process steps for fabricating n-channel and p-channel SiC gate FETs according to the present invention, including the fabrication of SiC floating gate transistors. The transistors can be produced on a silicon or other semiconductor substrate, an SOI substrate, or any other suitable substrate **108**. Only the process steps that differ from conventional CMOS process technology are described in detail.

In Figure **12A**, substrate **108** undergoes conventional CMOS processing up to the formation of the gate structure. For example, field oxide **1200** is formed for defining active regions **1202**. In a bulk semiconductor embodiment, well regions are formed, such as for carrying p-channel transistors.

In Figure **12B**, an insulating layer, such as thin oxide layer **118** or other suitable insulator, is formed on substrate **108**, such as by dry thermal oxidation, including over the portions of the active regions **1202** in which transistors will be fabricated. In one embodiment, thin oxide layer **118** is a gate oxide layer that can be approximately 100

angstroms (Å) thick. In another embodiment, such as in a floating gate transistor, thin oxide layer **118** is a tunnel oxide material that can be approximately 50 - 100 Å thick.

In Figure **12C**, a thin film **1206** of conductively doped polycrystalline or microcrystalline SiC is then deposited, such as by chemical vapor deposition (CVD) over the entire wafer, including over thin oxide layer **118**. The SiC composition x of film **1206** is differently selected according to the particular barrier energy desired at the interface between the gate **106** and adjacent thin oxide layer **118**, as described above. Microcrystalline SiC compounds may be selected for their lower electron affinity than polycrystalline SiC compounds in order to obtain the desired barrier energy.

The SiC film **1206** can be *in situ* doped during deposition, or doped during a subsequent ion-implantation step. The conductive doping can be n-type or p-type. In one light detecting embodiment, the SiC film **1206** is conductively doped n-type for enhanced photoelectric emission of electrons from floating gate **106** in response to incident light, as described above. In another embodiment, the SiC film **1206** is conductively doped p-type using a boron dopant, which advantageously diffuses from the SiC gate **106** less easily than from a polysilicon gate during subsequent thermal processing steps.

In one embodiment, for example, SiC film **1206** is deposited using low-pressure chemical vapor deposition (LPCVD), providing the structure illustrated in Figure **12C**. The LPCVD process uses either a hot-wall reactor or a cold-wall reactor with a reactive gas, such as a mixture of $Si(CH_3)_4$ and Ar. Examples of such processes are disclosed in an article by Y. Yamaguchi et al., entitled "Properties of Heteroepitaxial 3C-SiC Films Grown by LPCVD", in the 8th International Conference on Solid-State Sensors and Actuators and Eurosensors IX, Digest of Technical Papers, page 3. vol. (934+1030+85), pages 190-3, Vol. 2, 1995, and in an article by M. Andrieux, et al., entitled "Interface and Adhesion of PECVD SiC Based Films on Metals", in supplement Le Vide Science, Technique et Applications. (France), No. 279, pages 212-214, 1996. However, SiC film **1206** can be deposited using other techniques such as, for example, enhanced CVD techniques known to those skilled in the art including low pressure rapid thermal

chemical vapor deposition (LP-RTCVD), or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy (MBE). Other examples of forming SiC film **1206** include reactive magnetron sputtering, DC plasma discharge, ion-beam assisted deposition, ion-beam synthesis of amorphous SiC films, laser crystallization of amorphous SiC, laser reactive ablation deposition, and epitaxial growth by vacuum anneal. The conductivity of the SiC film **1206** can be changed by ion implantation during subsequent process steps, such as during the self-aligned formation of source/drain regions for the n-channel and p-channel FETs.

In Figure **12D**, SiC film **1206** is patterned and etched, together with thin oxide layer **118**, to form SiC gate **106**. SiC film **1206** is patterned using standard techniques and is etched using plasma etching, reactive ion etching (RIE) or a combination of these or other suitable methods. For example, SiC film **1206** can be etched by RIE in a distributed cyclotron resonance reactor using a SF_6 /O_2 gas mixture using SiO_2 as a mask with a selectivity of 6.5. Such process is known in the art and is disclosed, for example, in an article by F. Lanois, entitled "Angle Etch Control for Silicon Power Devices", which appeared in Applied Physics Letters, Vol 69, No. 2, pages 236-238, July 1996. Alternatively, SiC film **1206** can be etched by RIE using the mixture SF_6 and O_2 and F_2/Ar/O_2. An example of such a process is disclosed in an article by N. J. Dartnell, et al., entitled "Reactive Ion Etching of Silicon Carbide" in Vacuum, Vol. 46, No. 4, pages 349-355, 1955. The etch rate of SiC film **1206** can be significantly increased by using magnetron enhanced RIE.

Figure **12E** illustrates one embodiment in which SiC gate **106** is oxidized after formation, providing a thin layer **1210** represented by the dashed line in Figure **12E**. SiC gate **106** can be oxidized, for example, by plasma oxidation similar to reoxidation of polycrystalline silicon. During the oxidation process, the carbon is oxidized as carbon monoxide or carbon dioxide and vaporizes, leaving the thin layer **1210** of silicon oxide over SiC gate **106**. In one embodiment, thin layer **1210** is used as, or as a portion

of, an intergate dielectric between floating and control gates in a floating gate transistor embodiment of the present invention.

Figure **12F** illustrates generally a self-aligned embodiment of the formation of n-channel FET n+ source region **102** and drain region **104**. For a p-channel FET, p+ source drain regions can be similarly formed. The doping of SiC gate **106** can be changed by ion implantation, such as during the formation of n-channel FET or p-channel FET source/drain regions, or subsequently thereto. For example, a p-type SiC film **1206** can be deposited, and its doping then changed to n+ by leaving SiC gate **106** unmasked during the formation of the n+ source region **102** and drain region **104** for the n-channel FET.

Figure **12G** illustrates generally the formation of an insulating layer, such as oxide **114** or other suitable insulator, after formation of n-channel FET source region **102** and drain region **104**. In one embodiment, oxide **114** is deposited over the upper surface of the integrated circuit structure using a standard CVD process. Oxide **114** isolates SiC gate **106** from other gates such as, for example, an overlying or adjacent control gate layer **112** where SiC gate **106** is a floating gate in a floating gate transistor. Oxide **114** also isolates SiC gate **106** from any other conductive layer **112,** such as polysilicon layers, gates, metal lines, etc., that are fabricated above and over SiC gate **106** during subsequent process steps.

Conclusion

Thus, the invention includes a CMOS-compatible FET having a low electron affinity SiC gate that is either electrically isolated (floating) or interconnected. The SiC composition x is selected to provide the desired barrier at the SiC-SiO_2 interface, such as $0.5 < x < 1.0$. In a flash EEPROM application, the SiC composition x is selected to provide the desired programming and erase voltage and time or data charge retention time. In an imaging application, the SiC composition x is selected to provide sensitivity to the desired wavelength of light. Unlike conventional photodetectors, light is absorbed in the floating gate, thereby ejecting previously stored electrons therefrom.

Also unlike conventional photodetectors, the light detector according to the present invention is actually more sensitive to lower energy photons as the semiconductor bandgap is increased.

Although specific embodiments have been illustrated and described herein, those of ordinary skill in the art will appreciate that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.

WHAT IS CLAIMED IS:

1. A transistor comprising:

a source region, a drain region, a channel region between the source and drain regions, and a gate separated from the channel region by an insulator, the gate formed of a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a predetermined value approximately between 0 and 1.0 to establish a desired value of a barrier energy between the gate and the insulator.

2. The transistor of claim **1**, wherein the value of x is approximately between 0.5 and 1.0.

3. The transistor of claim **1**, wherein the value of the barrier energy is approximately between 0 eV and 2.8 eV.

4. The transistor of claim **1**, wherein the insulator is formed of silicon dioxide.

5. The transistor of claim **1**, wherein the gate is an electrically isolated floating gate and further comprising a control gate, separated from the floating gate by an intergate dielectric.

6. The transistor of claim **5**, wherein the intergate dielectric is formed of silicon dioxide.

7. The transistor of claim **5**, wherein the predetermined value x is selected to provide a desired charge retention time of the floating gate.

8. The transistor of claim **5**, wherein the predetermined value x is selected to provide a desired range of photon wavelengths most likely to be absorbed by the

floating gate whereby electrons are emitted from the floating gate in response to the absorbed photons.

9. The transistor of claim **8**, wherein the emission of electrons from the floating gate in response to incident photons changes a current conductance between the source and drain regions.

10. The transistor of claim **1**, wherein the gate is formed of a material selected from the group consisting of monocrystalline silicon carbide compound, a polycrystalline silicon carbide compound, a microcrystalline silicon carbide compound, and a nanocrystalline silicon carbide compound.

11. A device for detecting light, the device comprising:

a source region;

a drain region;

a channel region between the source and drain regions; and

a floating gate separated from the channel region by an insulator, the floating gate formed of a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a predetermined value approximately between 0 and 1.0 to establish a desired value of a barrier energy between the floating gate and the insulator for charge storage upon the floating gate and emission of charge from the floating gate in response to absorbed incident photons.

12. The device of claim **11**, further comprising a control gate located adjacent to the floating gate and separated therefrom by an interlayer dielectric.

13. The device of claim **11**, wherein x is selected at a predetermined value that is approximately between 0.5 and 1.0.

14. The device of claim **11**, wherein x is selected at a predetermined value to provide a desired value of the barrier energy that is approximately between 0 eV and 2.8 eV.

15. The device of claim **11**, wherein the predetermined value x is selected to provide a desired range of photon wavelengths most likely to be absorbed by the floating gate whereby electrons are emitted from the floating gate in response to the absorbed photons.

16. The device of claim **11**, wherein the emission of charge from the floating gate in response to incident photons changes a current conductance between the source and drain regions.

17. A memory device comprising:

a plurality of memory cells, wherein each memory cell includes a transistor comprising:

a source region;

a drain region;

a channel region between the source and drain regions;

a floating gate separated from the channel region by an insulator, the floating gate formed of a silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a predetermined value approximately between 0 and 1.0 to establish a desired value of a barrier energy between the gate and the insulator; and

a control gate located adjacent to the floating gate and separated therefrom by an interlayer dielectric.

18. The device of claim **17**, wherein the value of x is selected approximately between 0.5 and 1.0.

19. The device of claim **17**, wherein the value of the barrier energy is approximately between 0 eV and 2.8 eV.

20. The device of claim **17**, wherein the value of x is selected to provide a desired charge retention time of the floating gate.

21. A method of producing a transistor on a semiconductor substrate, the method comprising:

forming a source and drain regions, thereby defining a channel region between the source and drain regions;

forming an insulating layer on the channel region; and

forming a gate on the insulating layer, wherein the gate comprises a silicon carbide compound $Si_{1-x}C_x$; and

selecting x at a predetermined value approximately between 0 and 1.0.

22. The method of claim **21**, wherein x is selected to establish a desired value of a barrier energy between the gate and the insulator.

23. The method of claim **22**, wherein the selected value of x establishes the desired value of the barrier energy approximately between 0 eV and 2.8 eV.

24. The method of claim **21**, wherein x is selected at a predetermined value that is approximately between 0.5 and 1.0.

25. The method of claim **21**, wherein x is selected at a predetermined value that establishes a desired charge retention time.

26. The method of claim **25**, wherein the desired charge retention time is approximately between 1 second and 10^6 years.

27. The method of claim **21**, wherein the gate is a floating gate, and x is selected to provide a desired range of photon wavelengths most likely to be absorbed by the floating gate whereby electrons are emitted from the floating gate in response to the absorbed photons.

28. The method of claim **27**, wherein x is selected to provide sensitivity to light selected from the group consisting of infrared light, visible light, and ultraviolet light.

29. The method of claim **21**, wherein fabricating the gate includes the steps of :

depositing the silicon carbide compound using low pressure chemical vapor deposition to form a layer of gate material; and

etching the gate material to a desired pattern using a reactive ion etch process.

30. The method of claim **21**, wherein etching the gate material further includes using plasma etching in combination with the reactive ion etching.

31. The method of claim **21**, further comprising conductively doping the gate material prior to depositing the gate material on the insulating layer.

32. The method of claim **21**, further comprising oxidizing the gate material to form a thin layer of oxide on the gate material.

33. The method of claim **21**, wherein the gate is a floating gate, and further comprising:

forming a second insulating layer over the floating gate; and

forming a control gate over the second insulating layer.

34. An method of detecting light, the method comprising:

storing charge on a floating gate of a transistor;

receiving incident light at the floating gate, thereby removing at least a portion of the stored charge from the floating gate by the photoelectric effect; and

detecting a change in conductance between the transistor source and drain.

35. The method of claim **34**, further comprising selecting at least one wavelength of the incident light to which the floating gate transistor is most sensitive.

TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE

Abstract of the Disclosure

A CMOS-compatible FET has a reduced electron affinity polycrystalline or microcrystalline SiC gate that is electrically isolated (floating) or interconnected. The SiC material composition is selected to establish the barrier energy between the SiC gate and a gate insulator. In a memory application, such as a flash EEPROM, the SiC composition is selected to establish a lower barrier energy to reduce write and erase voltages and times or accommodate the particular data charge retention time needed for the particular application. In a light detector or imaging application, the SiC composition is selected to provide sensitivity to the desired wavelength of light. Unlike conventional photodetectors, light is absorbed in the floating gate, thereby ejecting previously stored electrons therefrom. Also unlike conventional photodetectors, the light detector according to the present invention is actually more sensitive to lower energy photons as the semiconductor bandgap is increased.

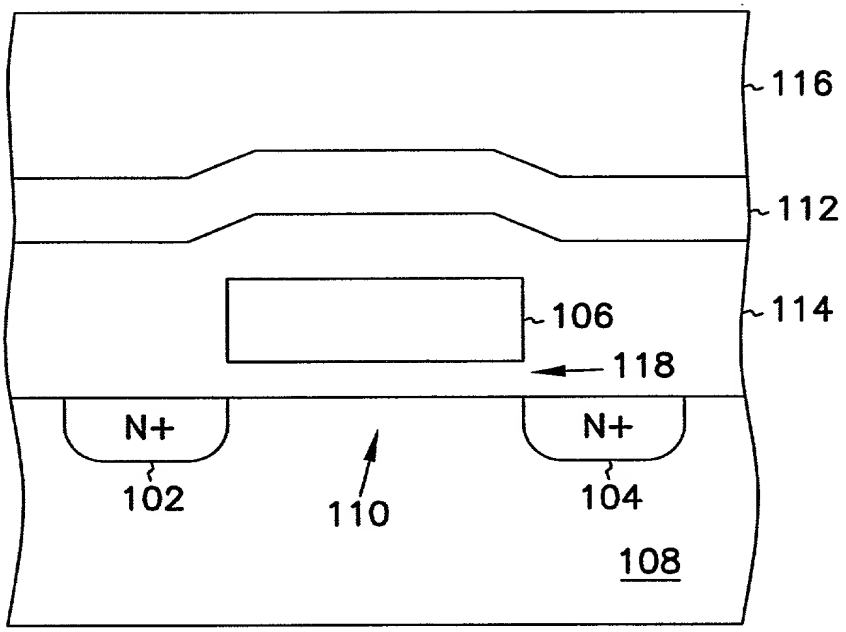
116
112
106
114
118
N+
N+
102
110
104
108

FIG. 1

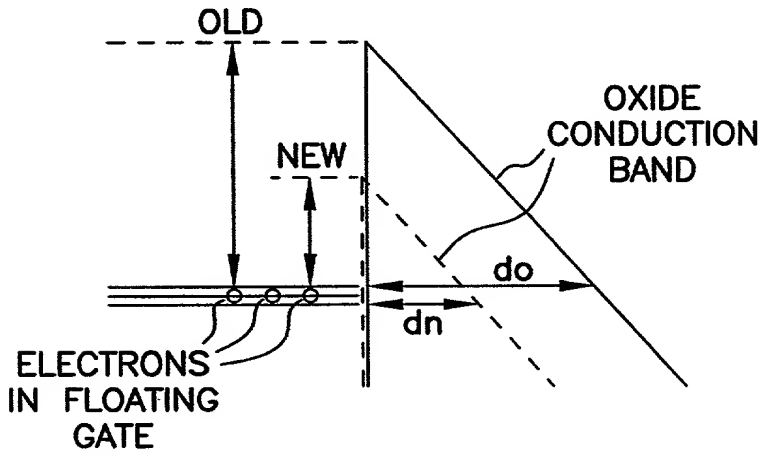
OLD
NEW
OXIDE
CONDUCTION
BAND
do
dn
ELECTRONS
IN FLOATING
GATE

FIG.2

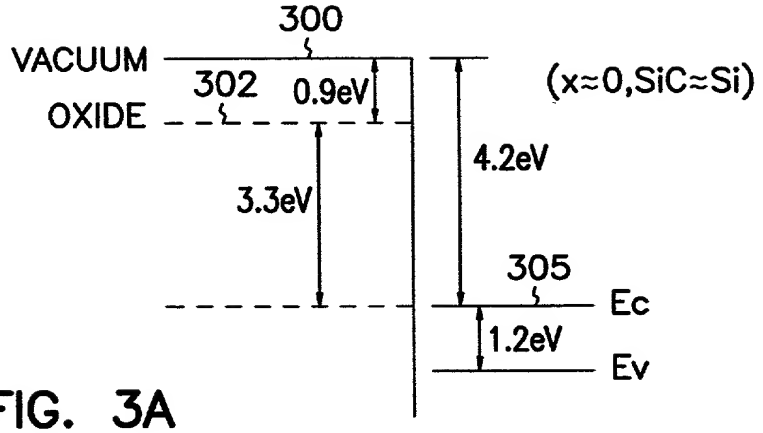

FIG. 3A

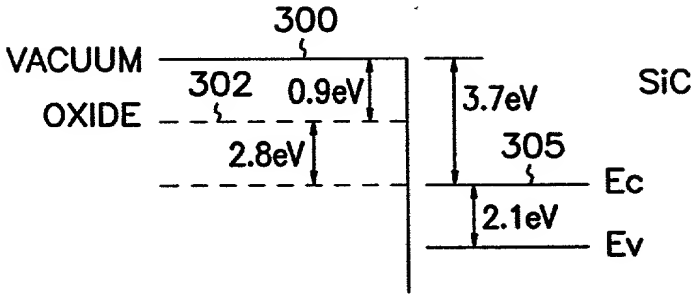

FIG. 3B

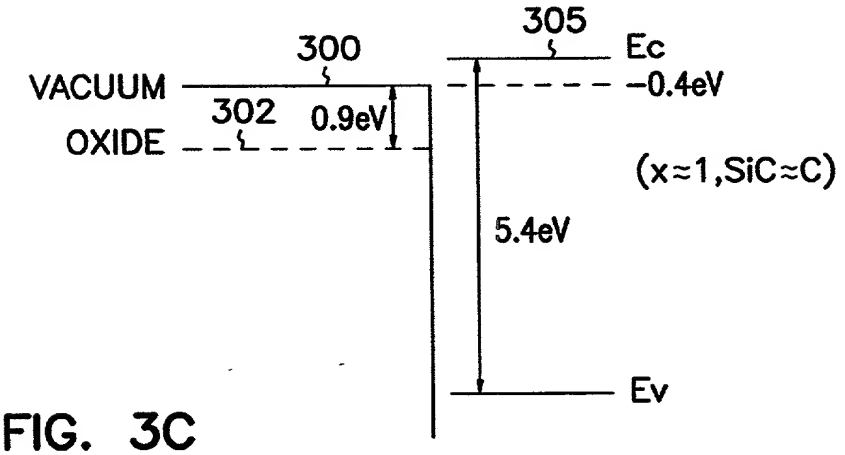

FIG. 3C

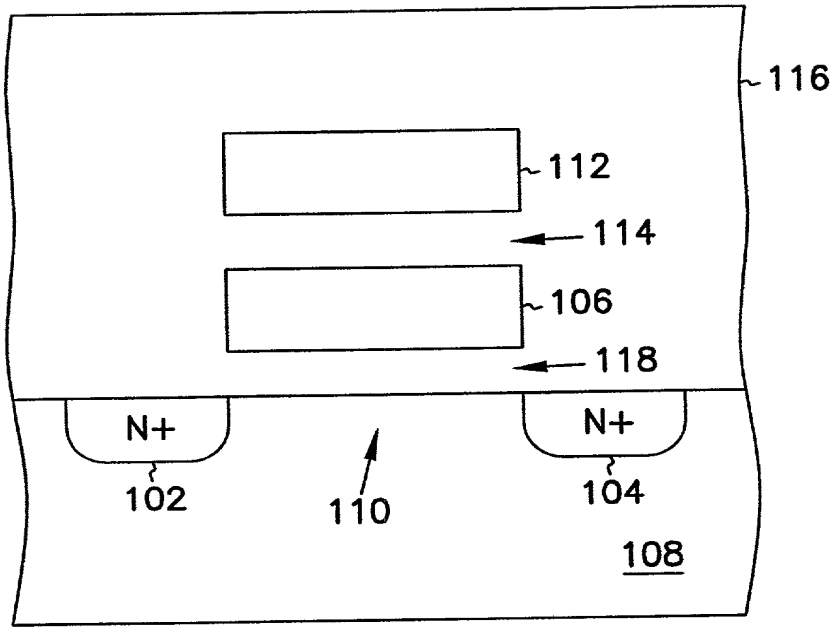

FIG. 4

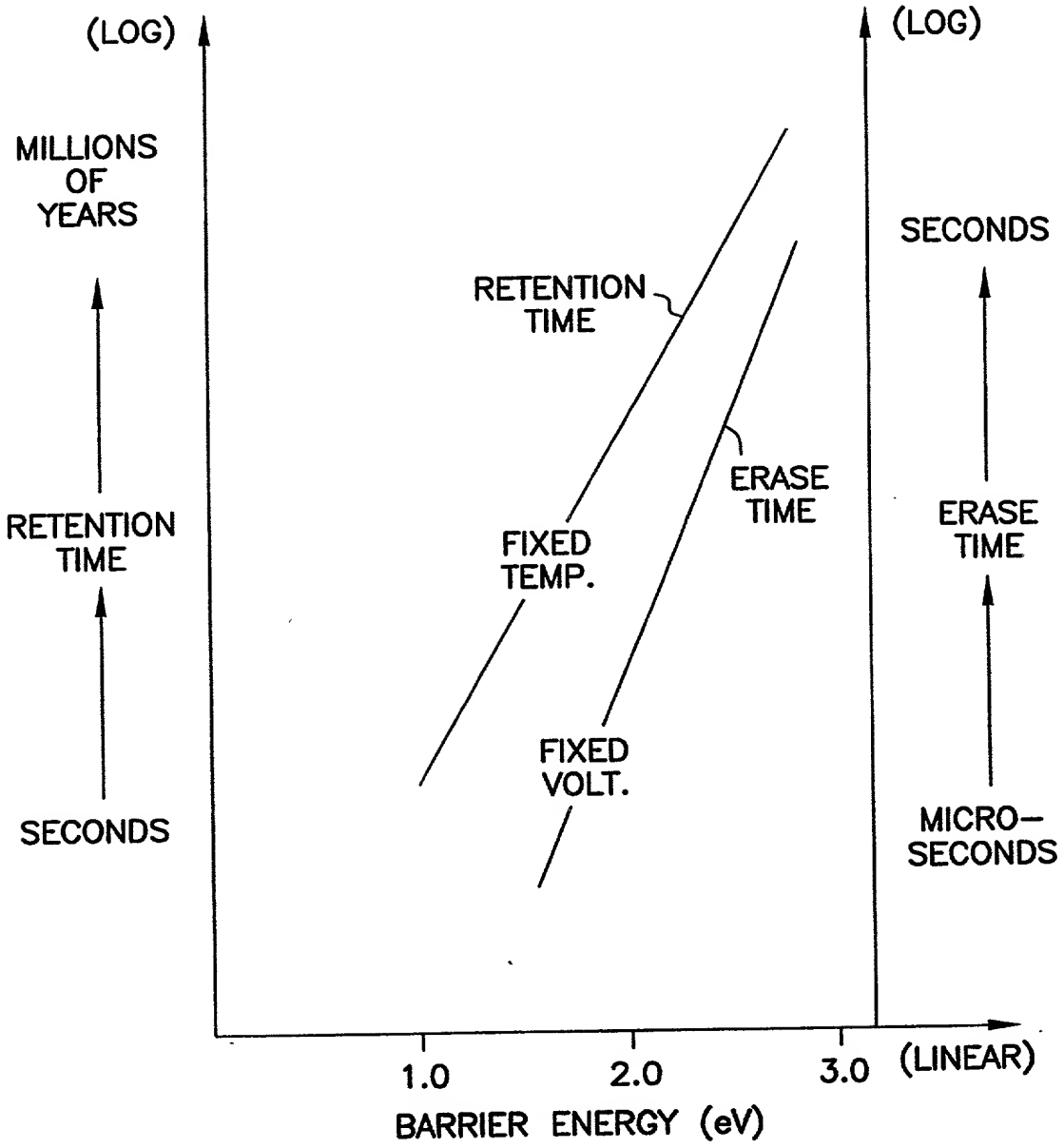
(LOG)
MILLIONS OF YEARS
RETENTION TIME
SECONDS
(LOG)
SECONDS
ERASE TIME
MICRO-SECONDS
RETENTION TIME
FIXED TEMP.
ERASE TIME
FIXED VOLT.
1.0
2.0
3.0
(LINEAR)
BARRIER ENERGY (eV)

FIG. 5

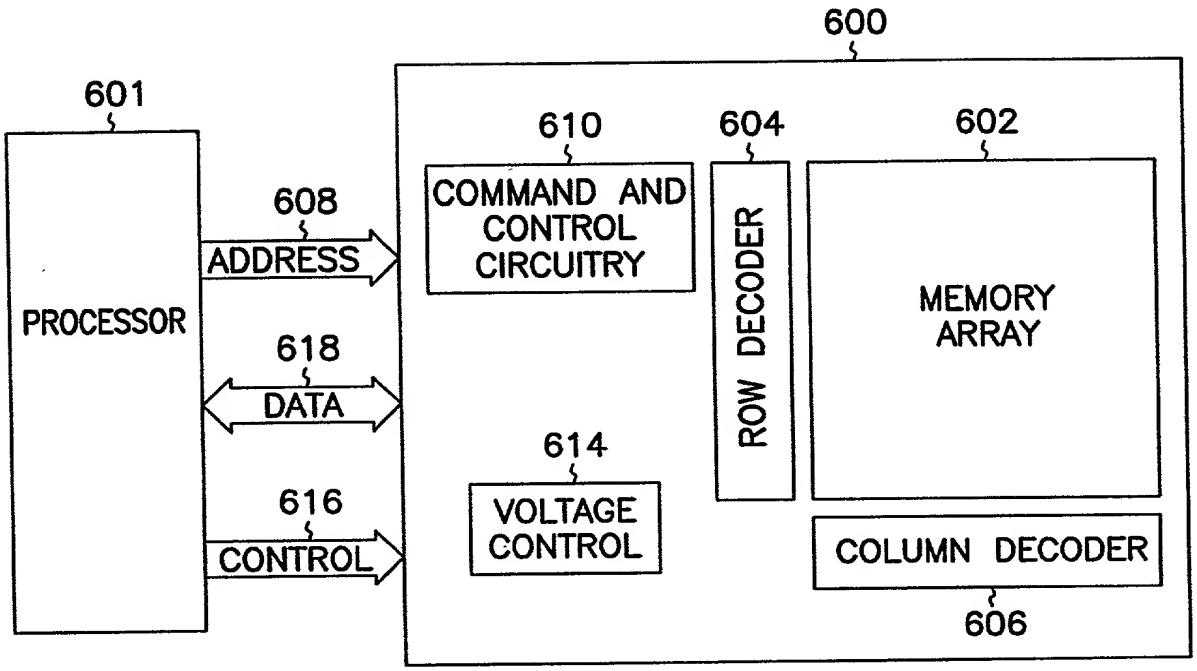
600
601
PROCESSOR
608
ADDRESS
618
DATA
616
CONTROL
610
COMMAND AND CONTROL CIRCUITRY
604
ROW DECODER
602
MEMORY ARRAY
614
VOLTAGE CONTROL
COLUMN DECODER
606

FIG. 6

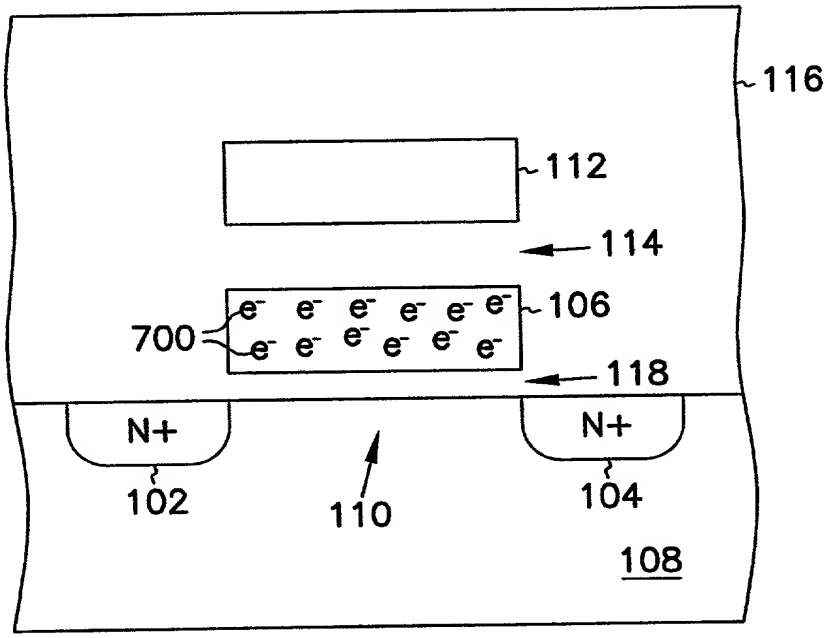
116
112
114
106
700
118
N+
N+
102
110
104
108

FIG. 7

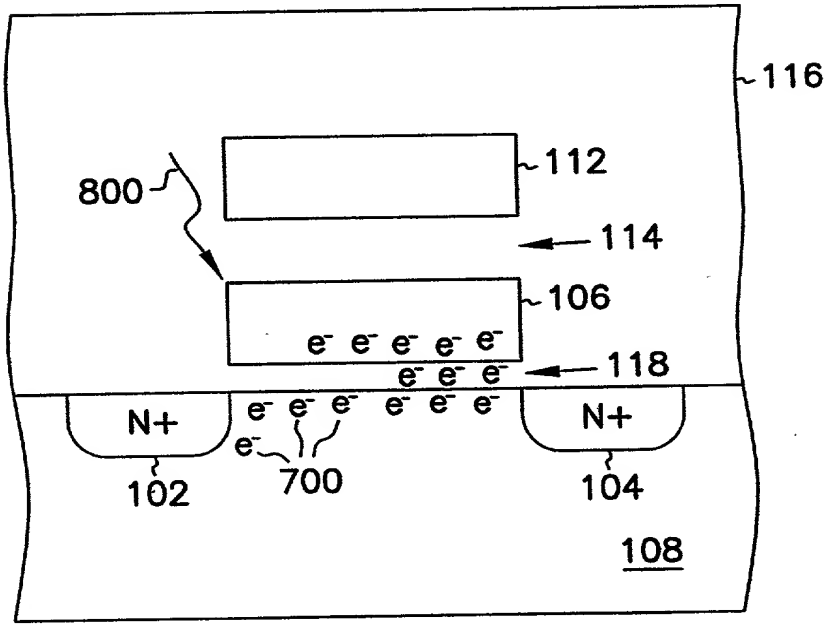
116
112
800
114
106
118
N+
N+
700
102
104
108

FIG. 8

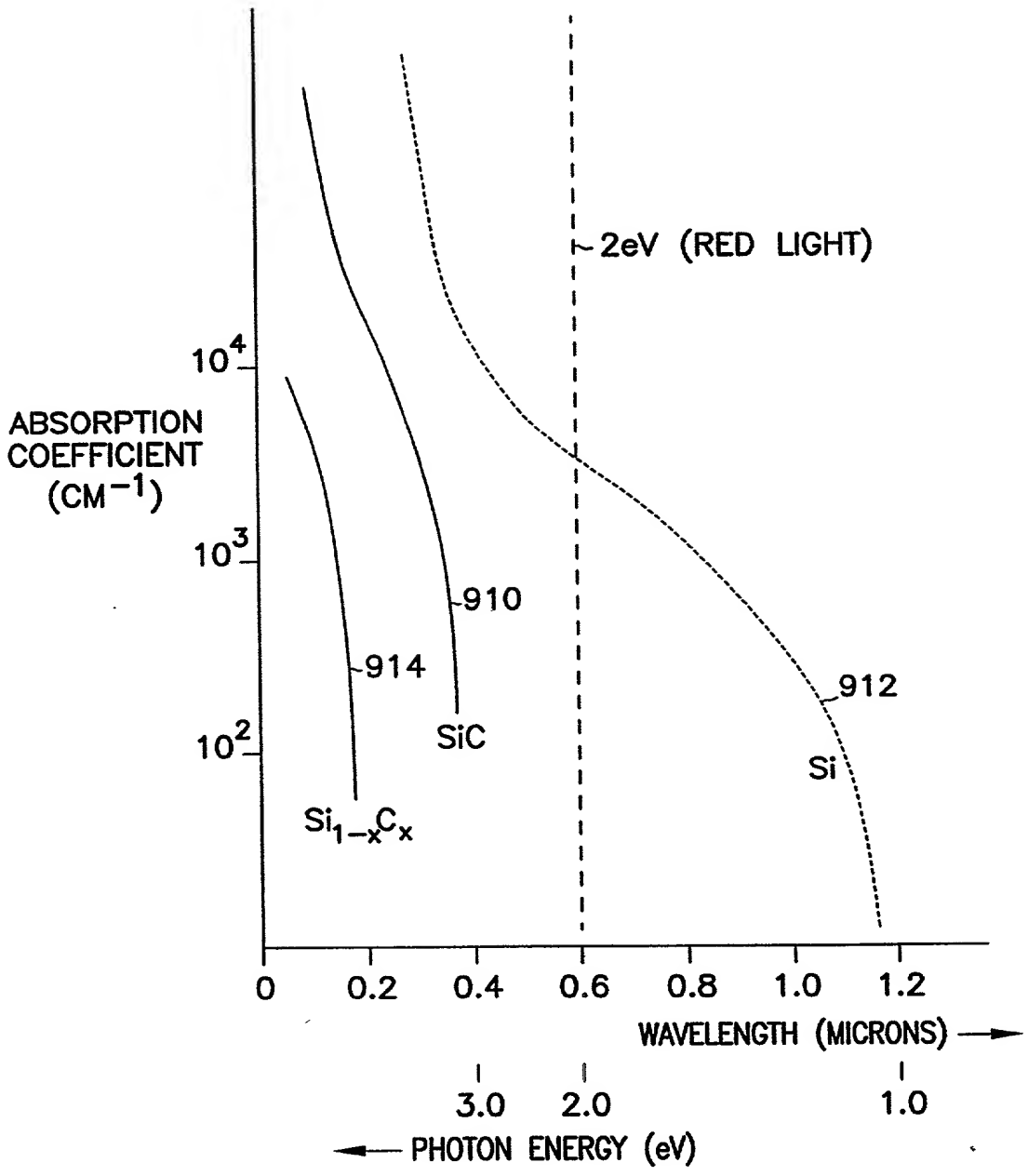
2eV (RED LIGHT)
10^4
10^3
10^2
ABSORPTION COEFFICIENT (CM^{-1})
910
914
912
SiC
Si
$Si_{1-x}C_x$
0
0.2
0.4
0.6
0.8
1.0
1.2
WAVELENGTH (MICRONS)
3.0
2.0
1.0
PHOTON ENERGY (eV)

FIG. 9

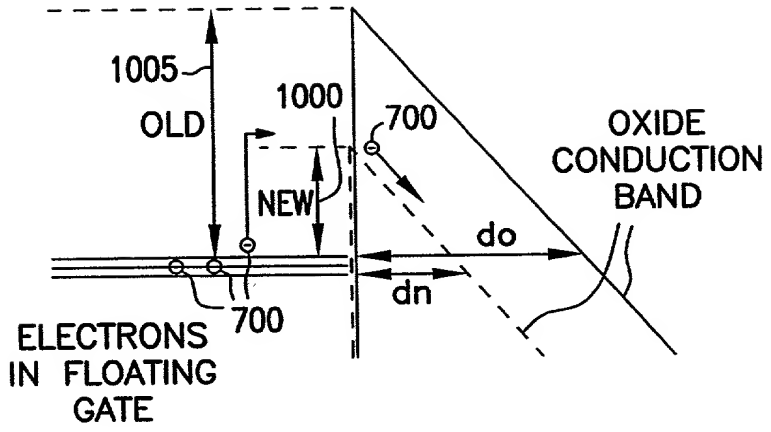
1005
OLD
1000
NEW
700
OXIDE
CONDUCTION
BAND
do
dn
700
ELECTRONS
IN FLOATING
GATE

FIG. 10

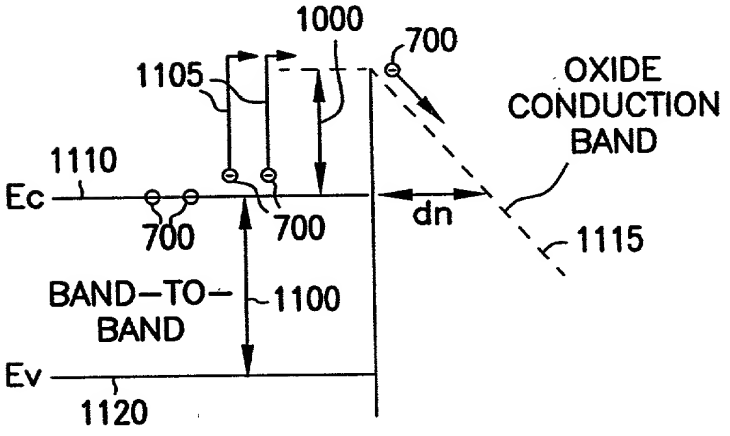
1000
700
1105
OXIDE
CONDUCTION
BAND
1110
Ec
dn
700
700
1115
BAND–TO–
BAND
1100
Ev
1120

FIG. 11

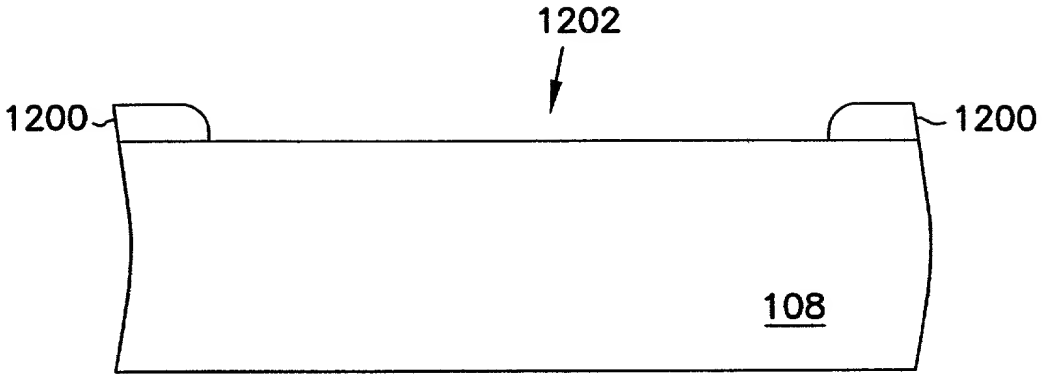

FIG. 12A

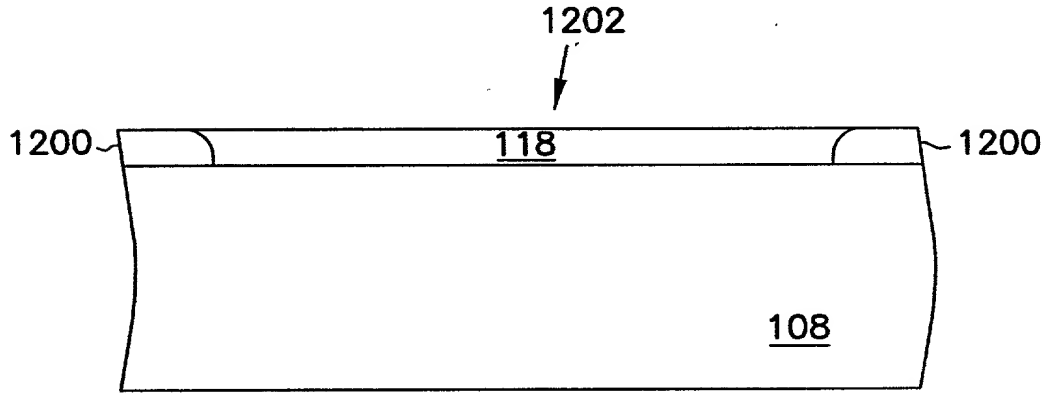

FIG. 12B

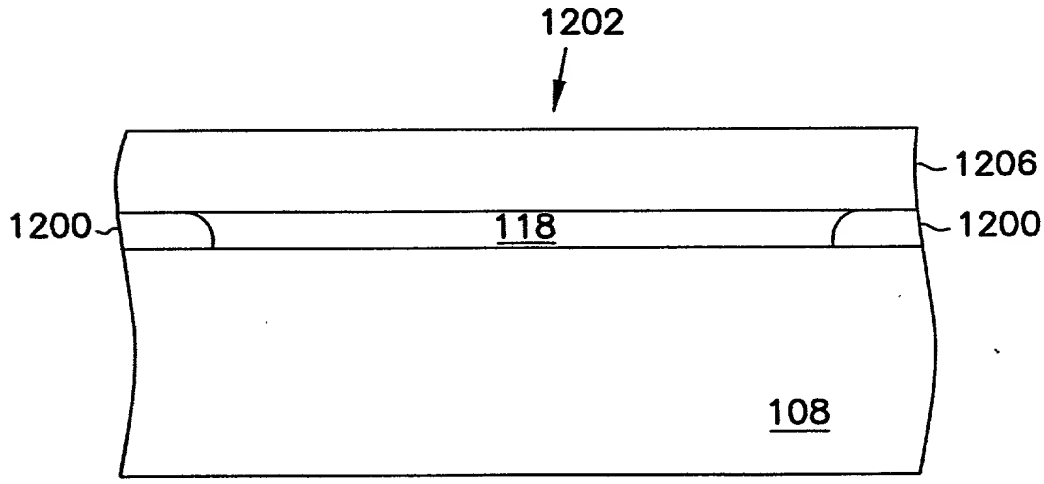

FIG. 12C

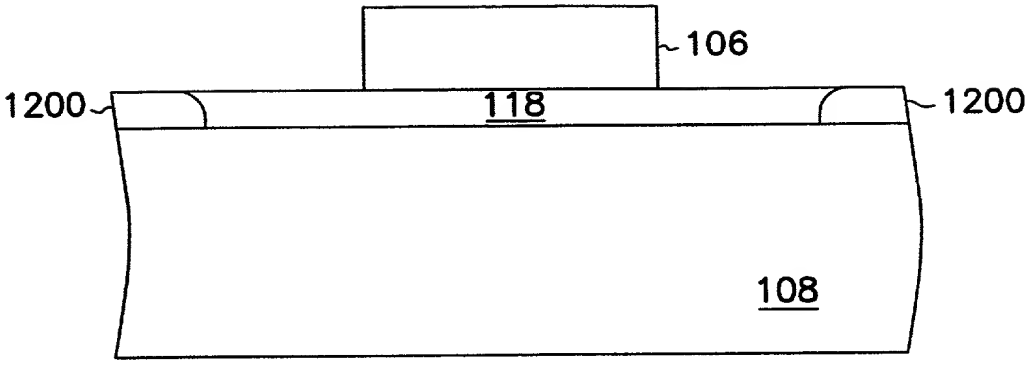

FIG. 12D

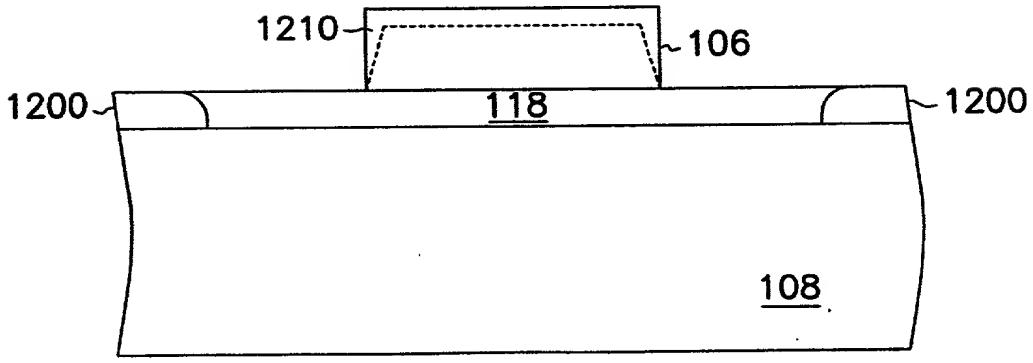

FIG. 12E

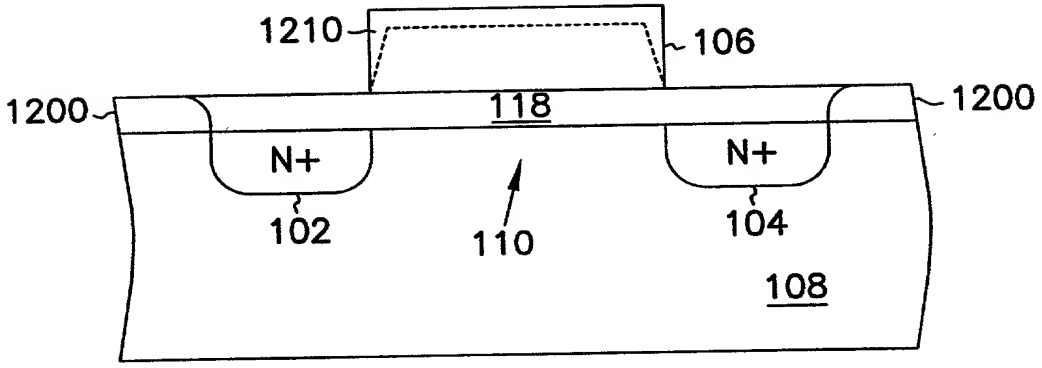

FIG. 12F

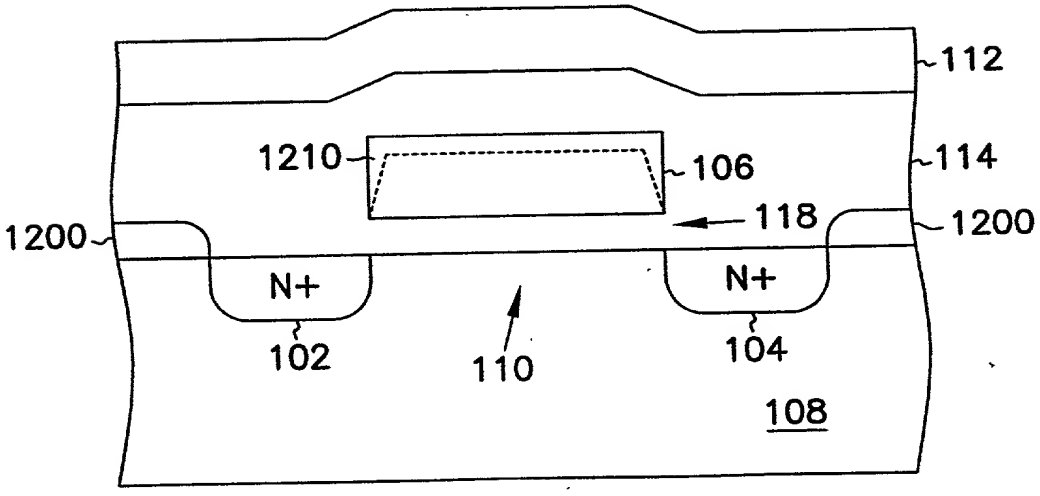

FIG. 12G

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE** .

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent of inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such applications have been filed.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

No such applications have been filed.

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

No such applications have been filed.

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

Bianchi, Timothy E.	Reg. No. 39,610	Fogg, David N.	Reg. No. 35,138	Lundberg, Steven W.	Reg. No. 30,568
Billig, Patrick G.	Reg. No. 38,080	Forrest, Bradley A.	Reg. No. 30,837	Lynch, Michael L.	Reg. No. 30,871
Billion, Richard E.	Reg. No. 32,836	Harris, Robert J.	Reg. No. 37,346	Pappas, Lia M.	Reg. No. 34,095
Brennan, Thomas F.	Reg. No. 35,075	Holloway, Sheryl S.	Reg. No. 37,850	Schwegman, Micheal L.	Reg. No. 25,816
Clark, Barbara J.	Reg. No. 38,107	Klima-Silberg, Catherine I.	Reg. No. 40,052	Simboli, Paul B.	Reg. No. 38,616
Dryja, Michael A.	Reg. No. 39,662	Kluth, Daniel J.	Reg. No. 32,146	Slifer, Russell D.	Reg. No. 39,838
Embretson, Janet E.	Reg. No. 39,665	Lemaire, Charles A.	Reg. No. 36,198	Viksnins, Ann S.	Reg. No. 37,748
Farney, W. Bryan	Reg. No. 32,651	Litman, Mark A.	Reg. No. 26,390	Woessner, Warren D.	Reg. No. 30,440

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/ firm/organization/who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Schwegman, Lundberg, Woessner & Kluth, P.A. to the contrary.

Please direct all correspondence in this case to Schwegman, Lundberg, Woessner & Kluth, P.A. at the address indicated below:

P.O. Box 2938, Minneapolis, MN 55402

Telephone No. (612)339-0331

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of joint inventor number 1 : **Leonard Forbes**
Citizenship: **United States of America** Residence: **Corvallis, OR**
Post Office Address: 965 NW Highland Terrace
Corvallis, OR 97330

Signature: _____ Date: 16 June 97
Leonard Forbes

Full Name of joint inventor number 2 : **Kie Y. Ahn**
Citizenship: **United States of America** Residence: **Chappaqua, NY**
Post Office Address: 639 Quaker St.
Chappaqua, NY 10514

Signature: _____ Date: _____
Kie Y. Ahn

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE**.

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent of inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such applications have been filed.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

No such applications have been filed.

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

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Post Office Address: 965 NW Highland Terrace
Corvallis, OR 97330

Signature: _____ Date: _____
Leonard Forbes

Full Name of joint inventor number 2 : **Kie Y. Ahn**
Citizenship: **United States of America** Residence: **Chappaqua, NY**
Post Office Address: 639 Quaker St.
Chappaqua, NY 10514

Signature: Kie Y. Ahn Date: June 18, 1997
Kie Y. Ahn

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
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